ECEN 429: Introduction to Digital Systems Design Laboratory

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Pre Lab #5

**Introduction**

The prelab for lab5 is focused around studying vhdl codes with nand and xnor gates, knowing how components work, and an introduction to Flip flops and SR latches. The prelab will help us to get a better understand before we attempt to complete the lab and a better understanding into the concepts of digital systems.

**Background, Design Solution and Results**

The prelab provided us with analyzing blocks of code, figuring out what the outputs of a D flip flop would be, and using an SR latch to come up with a truth table and code for the device.

Problem 1:

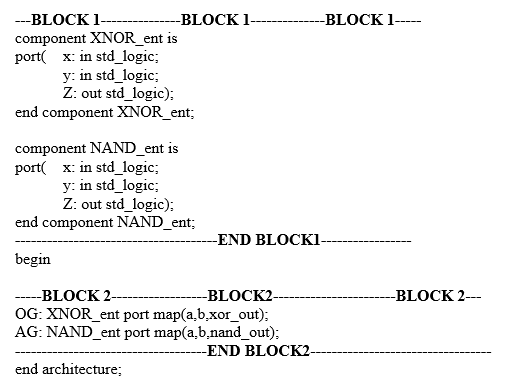


Figure 1.1 this is the block of code needed to be analyzed for problem 1.

Above is the code asked to be analyzed in the prelab. The first block of code we have components being made. Components can be put together to make bigger more functional devices. The second block of code are the port maps where all those components can connect.

Problem 2:

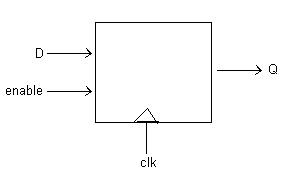


Figure 2.1 The figure of a D flipflop

The problem asks what line of code gives a positive edge triggered characteristic. The answer is B which is “If (clk’event) and (clk = ‘1’) then”. This will mean if the clock event is going to happen and the clk is high then.. do something. The D flip flop works as a clock and has an enable that allows it to get triggered. It is pivotal in state machines and other devices that might have some time component to them in digital systems.

|  |  |  |  |
| --- | --- | --- | --- |
| Clk | D | Q | Q’ |
| 0 | 0 | Q | Q’ |
| 0 | 1 | Q | Q’ |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Table 1.1 This is a truth table of a D flipflop

The code for the D flip flop would be roughly this:

Entity D is

Port Q: out

Clk,D, in }

End

Arch beh of D is

Begin

Process clk

Begin

If (clk event’ and if clk=1) then Q<=D;

End if

End

end

Problem 3

Problem 3 of the prelab was all about SR latches. We were asked to provide a truth table for the SR latch as well as some code for the latch.

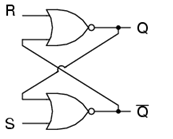


Figure 3.1 This is the image of a SR latch

|  |  |  |  |
| --- | --- | --- | --- |
| S | R | Q | Q’ |
| 0 | 0 | Latch | Latch |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

Table 3.1 Truth table of a SR latch

The code for an SR would be similar to:

Entity SR is

Port (S,R in

Q,Qnot: out

End

Arch bev of SR is

Begin

Q3<= Qnot nor R

Qnot<= Q3 nor S

end

**Conclusion**

After doing the prelab, I understand SR latches and D flip flops a lot better. This will come in helpful when we start to do the lab this week based around these two subjects.